REMARKS/ARGUMENTS

Claims 1-34 were pending. Upon entry of this amendment amending claims 1, 2 18, and 30, claims 1-34 remain pending. Claims 1, 2, 4-8, 18, 19, 22, 23, and 28-34 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,385,213 issued to Nakamura et al. (hereinafter "Nakamura"). Under 35 U.S.C. 103(a) Claim 3 stands rejected in view of Nakamura, and claim 20 stands rejected as being unpatentable over Nakamura in view of U.S. Patent No. 6,359,908 issued to Soda (hereinafter "Soda"). Applicants aver that no new matter has been added in this response.

§102/§103 Rejections

Claims 1, 18, and 30

In the Office Action, the Examiner rejected claims 1, 2, 4-8, 18, 19, 22, 23, and 28-34 under 35 U.S.C. §102(e) as being anticipated by Nakamura, and under 35 U.S.C. §103(a) the Examiner rejected claim 3 as being obvious in view of Nakamura and claim 20 as being obvious in view of Nakamura in further view of Soda.

Regarding claim 1, the Examiner states that Nakamura teaches a method for detecting a boundary between two bytes X1 and X2 in a deserialized data stream, where the data stream includes N consecutive X1 bytes followed by N consecutive X2 bytes, where the method includes storing a first M bytes of data, where M is smaller than N, monitoring at least a subsequent second M bytes of data, comparing each of the first M bytes to a value X I *, comparing each of the second M bytes to a value X2*, where X1 * represents X1 or any value resulting from a bit shift of XI, wherein X2* represents X2 or any value resulting from a bit shift of X2, where the X1X2 boundary bytes is detected when each of the first M bytes equals X I *, and each of the second M bytes equals X2* point to col. 10 and figs. 3, 4, 14, and 33, and col. 1 and col. 10, et seq. of Nakamura.

Regarding claim 18, in the Office Action, the Examiner states that Nakamura teaches A SONET data processor which include a first register coupled to an input SONET data bus, a comparator having at least a first input coupled to the input data bus and a second input

coupled to the first register such that the comparator has substantially simultaneous access to paralleled data associated with two successive clock cycles, where the comparator compares the values in some portion of the input data bus with a predetermined value, and wherein the comparator compares the values in some portion of the first register with a predetermined value. In the Office Action, the Examiner states that Nakamura teaches a SONET (SDH) line card having a transceiver configured to deserialize data into a plurality of parallel data streams, a framer used to detect a A1A2 boundary, a network processing unit, pointing to figs. 3, 4, 6, 10, 18, and fig. 28-30, 32a, 33 et seq. of Nakamura. In the Office action, the Examiner states that Soda discloses a second register pointing to Fig. 2 *et seq.* of Soda.

Regarding claim 30 in the Office Action, the Examiner states Nakamura teaches a method of processing data in a SONET frame where the method includes receiving first and second consecutive N bytes of data (m), comparing N/2 consecutive bytes of the first N bytes of data with a first predetermined pattern defined by the Al byte in a SONET frame header, comparing N/2 consecutive bytes of the second N bytes of data with a second predetermined pattern defined by the A2 byte in a SONET frame header; if a match is found in both compare steps, forming a third consecutive N+1 bytes by combining the two N/2 consecutive bytes of data plus one additional byte, shifting data bits in each byte of the third consecutive N+1 bytes so that each byte corresponds to an AI or an A2 byte, and shifting the AI and M bytes to align N consecutive bytes along the AM2 boundary pointing to figures 6-8 *et seq.* of Nakamura. Applicants respectfully traverse the rejections.

Applicants submit that Nakamura or Soda alone or in combination do not disclose all of the elements of claims 1, 18, or 30. For example, amended claim 1 partially recites "a method for detecting a boundary between two bytes X1 and X2 in a deserialized data stream... storing a first M bytes of data, where M is smaller than N...monitoring at least a subsequent second M bytes of data, *wherein the first M bytes of data and the second M bytes of data are from sequential segments of [a] deserialized data stream*", and claim 18 as amended partially recites "a comparator having at least a first input coupled to [an] input data bus and a second input coupled to [a] first register such that the comparator has substantially simultaneous access to paralleled data associated with *two successive clock cycles...wherein [] values in some*

portion of the input data bus and [] values in some portion of the first register are from sequential segments of a deserialized data stream", and claim 30 as amended partially recites "a method of processing data in a SONET frame...receiving first and second consecutive N bytes of data, *wherein the first N bytes of data and the second N bytes of data are from sequential segments of a deserialized data stream*" (emphasis added).

Nakamura discloses a A1A2 boundary detection system that uses a data switch to arrange parallel data such that a synchronous frame pattern comes at the start of the parallel data. In Nakamura, parallel data is provided to a temporary frame synchronous pattern detection section which is used to detect a candidate region where the A1A2 boundary is most likely located. The temporary frame synchronous pattern detection section then serializes the parallel data and feeds the serialized data to a frame synchronous detection section to detect the A1A2 pattern. The temporary frame synchronous pattern detection section uses a A1 byte detection section and a A2 byte diction section that receive simultaneous parallel data input. After A2 is detected by the A2 detection section after A1 is detected by the A1 detection section, a range of bytes before and after are latched. The output of the latch is serially delivered to the frame synchronous detection section to detect the A1A2 pattern. In other words, Nakamura processes a parallel word to locate a given portion of the word were the A1A2 boundary might be located, and then uses another process to detect the A1A2 pattern in the suspect portion of the word. As the actual position of A1 is unknown, the A2 pattern is used to establish the region pf data that should contain both A1 and A2, the process of which can take several clock cycles.

Nakamura does not disclose a method for detecting a boundary between two bytes in a deserialized data stream, where a first set of data and a subsequent second of data are *from sequential segments of the deserialized data stream*, or a comparator having a first input coupled to an input data bus and a second input coupled to a first register where *values of a portion of the input data bus and values of a portion of the first register are from sequential segments of a deserialized data stream*, or a method of processing data in a SONET frame including receiving first and second consecutive N bytes of data *where the first N bytes of data and the second N bytes of data are from sequential segments of a deserialized data stream* as claimed. On the contrary, Nakamura discloses a A1A2 detection process that first detects a region of parallel data

that the A1A2 boundary may be located in, and then *serializes* the detected region of the paralle data so that a second circuit can more efficiently locate the A1A2 boundary within the detected region (emphasis added) (See Nakamura, Figs. 3-6, col. 14, line 13 through col. 15 line 27, and col. 15, line 40 through col. 16 line 67). Soda discloses a frame synchronous circuit that includes a A1-byte detecting circuit, a first register, and a second register. In Soda, the first and second registers are used for deserilizing a serial input signal, and inputting two of the same byte of data of the deserilized signal, offset by one bit, into the A1-byte detection circuit (See Soda, fig. 2, col. 2 lines 10-30). Therefore Applicants submit that Soda fails to make up for what Nakamura lacks.

Therefore, as claims 1, 18, and 30 disclose elements not disclosed by Nakamura and Soda, taken alone or in combination, Applicants submit claims 1, 18, and 30 are allowable.

Dependent claims 2-8, 19-29, and 31-34

Claims 2-8 which depend from claim 1, claims 19-29 which depend from claim 18, and claims 31-34 which depend from claim 30 are allowable for at least the reasons discussed in relation to claims 1, 18, and 30, as well as the limitations they recite.

Allowed Claims

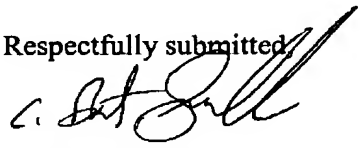
Applicants appreciate the allowance of claims 9-17.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,



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